Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (currently amended) An apparatus comprising:

a plurality of transmission circuits to transmit data over one or more of a set of output lines;

a plurality of receiving circuits to receive ~~data~~ bits over one or more of a set of output lines; and

a plurality of parallel-serial conversion circuits coupled to the plurality of transmission circuits and to the plurality of receiving circuits, the plurality of conversion circuits ~~to~~ operable to:

convert a parallel ~~signals~~ signal to ~~one ore more sets of~~ multiple serial signals including the received bits and ~~to~~ send the converted serial signals to one or more corresponding transmission circuits, and ~~to~~

receive one or more sets of serial signals from one or more of the receiving circuits and ~~to~~ convert the serial signals to parallel signals,[.]

wherein:

stuffing data is added to the received bits in the multiple serial signals such that the number of the multiple serial signals multiplied by the second bit rate is equal to the first bit rate,

at least one of the plurality of parallel-serial conversion circuits receives SONET/SDH framed data at a first bit rate as a parallel signal and converts the parallel signals to multiple serial signals at a second bit rate, where the first bit rate is different than the second bit rate, and

the corresponding transmission circuit transmits the multiple serial signals at the second bit rate.

Cont A'

2. (currently amended) The apparatus of claim 1 further comprising a control circuit coupled to the plurality of transmission circuits, to the plurality of receiving circuits and to the plurality of parallel-serial conversion circuits, the control circuit to ~~control~~ control conversion of signals between parallel and serial formats and to control transmission and receiving of data.

3. (currently amended) The apparatus of claim 1, wherein at least one of the plurality of parallel-serial conversion circuits receives SONET/SDH framed data at a first ~~data~~ bit rate as a parallel signal and converts the parallel signal to a corresponding serial signal at the first ~~data~~ bit rate.

4. (currently amended) The apparatus of claim 3, wherein one of the plurality of transmission circuits transmits the converted serial signal at the first ~~data~~ bit rate.

Claims 5-6 (canceled)

7. (currently amended) The apparatus of claim 1, wherein at least one of the plurality of parallel-serial conversion circuits receives a serial signal at a first ~~data~~ bit rate and converts the serial signal to a parallel SONET/SDH framed data at the first ~~data~~ bit rate.

8. (currently amended) The apparatus of claim 7, wherein one of the plurality of receiving circuits receives the serial signal at the first ~~data~~ bit rate and sends the serial signal to the parallel-serial conversion circuit.

9. (currently amended) The apparatus of claim 1, wherein one of the plurality of parallel-serial conversion circuits receives multiple serial signals at a first ~~data~~ bit rate and converts the serial signals to parallel SONET/SDH framed data at a second ~~data~~ bit rate, where the second ~~data~~ bit rate is greater than the first ~~data~~ bit rate.

10. (currently amended) The apparatus of claim 9, wherein one of the receive circuits receives the multiple serial signals at the first ~~data~~ bit rate.

11. (currently amended) A method comprising:

receiving bits in a parallel signal at a first rate;

converting the parallel signal into multiple serial signals; and

transmitting the multiple serial signals including the received bits at a second bit rate, the second bit rate being different than the first bit rate,[.]

wherein stuffing data is added to the received bits in the multiple serial signals such that the number of the multiple serial signals multiplied by the second bit rate is equal to the first bit rate, and

wherein the bits are received as SONET/SDH framed data in the parallel signal.

Claims 12-13 (canceled)

14. (currently amended) The method of claim 11 further comprising transmitting the multiple serial signals at the second bit rate ~~with~~ using both a first transmitting circuit and ~~with a~~ second transmitting circuit.

15. (currently amended) A method comprising:

receiving bits in multiple serial signals at a first bit rate;

converting the multiple serial signals to a parallel signal;

transmitting the parallel signal including the received bits at a second bit rate, wherein the second bit rate is greater than the first bit rate,[.]

wherein stuffing data is removed from at least one of the multiple serial signals during conversion such that the number of the multiple serial signals multiplied by the first bit rate is equal to the second bit rate, and

wherein the bits are SONET/SDH framed data in the parallel signal.

Claims 16-17 (canceled)

18. (currently amended) The method of claim 15 further comprising receiving the multiple serial signals at the first bit rate ~~with~~ using both a first receiving circuit and ~~with~~ a second receiving circuit.

19. (currently amended) An apparatus comprising:

means for receiving bits of a parallel signal at a first rate;

means for converting the parallel signal into multiple serial signals; and

means for transmitting the multiple serial signals including the received bits at a second bit rate,[.] the second bit rate being different than the first bit rate,

wherein stuffing data is added to the received bits in the multiple serial signals such that the number of the multiple serial signals multiplied by the second bit rate is equal to the first bit rate, and

wherein the bits are received as SONET/SDH framed data in the parallel signal.

Claims 20-21 (canceled)

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22. (currently amended) The method of claim 19 further comprising means for transmitting the ~~multiple~~ serial signals at the second bit rate ~~with~~ using both a first transmitting circuit and ~~with~~ a second transmitting circuit.

23. (currently amended) An apparatus comprising:

means for receiving bits in multiple serial signals at a first bit rate;

means for converting the multiple serial signals to a parallel signal;

means for transmitting the parallel signal including the received bits at a second bit rate, wherein the second bit rate is greater than the first bit rate[.],

wherein stuffing data is removed from at least one of the multiple serial signals during conversion such that the number of the multiple serial signals multiplied by the first bit rate is equal to the second bit rate, and

wherein the received bits are transmitted as SONET/SDH framed data in the parallel signal.

Claims 24-25 (canceled)

26. (currently amended) The apparatus of claim 23 further comprising receiving the multiple serial signals at the first bit rate ~~with~~ using both a first receiving circuit and ~~with~~ a second receiving circuit.

27. (New) The apparatus of claim 1, wherein
the first bit rate corresponds to an STS-48 line rate,
the second bit rate corresponds to an STS-12 line rate, and
the number of transmitted serial signals is four.

28. (New) The apparatus of claim 11, wherein
the first bit rate corresponds to an STS-48 line rate,
the second bit rate corresponds to an STS-12 line rate, and
the number of transmitted serial signals is four.

29. (New) The apparatus of claim 15, wherein
the first bit rate corresponds to an STS-12 line rate,
the second bit rate corresponds to an STS-48 line rate, and
the number of received serial signals is four.

30. (New) The apparatus of claim 19, wherein
the first bit rate corresponds to an STS-48 line rate,
the second bit rate corresponds to an STS-12 line rate, and
the number of transmitted serial signals is four.

31. (New) The apparatus of claim 15, wherein
the first bit rate corresponds to an STS-12 line rate,
the second bit rate corresponds to an STS-48 line rate, and
the number of received serial signals is four.